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| EXAMINER | |
|---|---|
| GOSSAGE, GLENN A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2187 | 20 |

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/401,765 | CALAMATAS, PHILIP J. | |
| | Examiner | Art Unit | |
| | Glenn Gossage | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05-03-04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The abstract of the disclosure is objected to because it does not enable one to quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b). It appears one or two sentences should be (re)inserted describing additionally claimed and disclosed features. [For example, in line 19, after "circuit.", (re)insert a sentence such as --The tri-state data bus may be connected between a digital signal processor (DSP), a complex programmable logic device (CPLD) and a central processing unit (CPU) operating at different rates or speeds.-- . See claims 12 and 13, e.g.]

Appropriate correction is required. See MPEP § 608.01(b).

2. The proposed drawing corrections filed on May 3, 2004 have been DISAPPROVED by the Examiner as possibly containing NEW MATTER.

For example, in Figure 5, the placement of the data bus memory buffer circuitry 220 within the CPU card 200 does not appear to be consistent with the disclosure as originally filed (including material incorporated by reference) and may constitute new matter.

Also, the addition of a dashed "box" 318 within "box" 300 does not appear to be entirely consistent with the originally filed disclosure. [It appears the dashed "box" and associated reference numeral 318 should be deleted, and "300" changed to --MC-CPLD 318 (on MD- I/O Card 300)-- for clarity and consistency (note the proposed drawing corrections filed October 27, 2003, as well as pages 9-10 of the response filed May 3, 2004, particularly page 9, lines 19-23). Additionally, it appears "box" 321 should be changed back to --320--, and a label such as --(on MD- I/O Card 300)-- reinserted within "box" 320, for clarity and consistency. Again see the

proposed drawing corrections filed October 27, 2003, and note that CPLDs 318 and 316 and DSP 320 are located on MD- I/O card 300.] The deletion of the feedback 366 and associated lines/circuits without explanation is also not understood and may constitute mew matter.

The proposed drawings are also objected to because in Figure 4, the use of the same reference numeral (340, e.g.) for different elements is confusing and improper. See 37 CFR 1.84(f), and also note the insert beginning with the paragraph spanning pages 15-16 through the paragraph spanning pages 21-22 (as shown in the amendment filed May 3, 2004), referring to seven segment display 340 (first paragraph of the insert, at line 6) and push back position switches 340 (third line from the end of the insert). It is also not entirely clear to what "CRDL" refers within block 320. Should "CRDL CHIPS" be changed to simply --CHIP--?

The remaining changes shown in the proposed drawing corrections filed are acceptable (except that black ink should be used in the formal drawings), but should be resubmitted for proper approval and entry by the examiner.

Applicant is again REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

3. It is once again noted here that the specification, particularly the material added or incorporated from the provisional application, has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

In the paragraph bridging pages 6 and 7 (as shown in the amendment filed May 3, 2004), at line 8 of the paragraph, it appears "in block" should be deleted for clarity and consistency with the disclosure as originally filed and to avoid any possible questions of new matter. Similarly, at line 9 of the paragraph, it appears "also in block 320" should be changed back to --300-- for clarity and consistency with the disclosure as originally filed and avoid possible questions of NEW matter.

In the amended insert or passage substituted for the paragraphs beginning with the paragraph bridging pages 15 and 16 through the paragraph bridging pages 21 and 22, at lines 3 and 4 of the insert, it appears "(also) in block 320" should be deleted for clarity and consistency with the disclosure as originally filed and avoid possible questions of NEW MATTER, analogous to the paragraph bridging pages 6 and 7 discussed above. Similarly, in lines 7 and 13 of the passage, respectively, it appears "in block 320" and "in block" should be deleted for clarity and consistency. Also, in line 6 of the paragraph, the use of the same reference numeral (340) for different elements is confusing (also see the third line from the end of the insert, for example).

In the paragraph beginning "Figures 4 and 5 best illustrate ..." (see page 11 of the amendment), the deletion of the three sentences referring to the FETs and feedback 366 without explanation is not understood and may constitute a change in scope of the disclosure and thus new matter. It appears the sentence should be reinserted for clarity and consistency.

Also, it appears the reference numerals 410-430 shown in Figure 4 should be discussed or mentioned, at least briefly, for clarity and completeness, since it does not appear these reference numerals or elements are presently discussed anywhere in the specification.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 12, line 5, it appears --(DSP)-- should be inserted after "Processor" for clarity.

Similarly, in claim 13, line 4, it appears --(CPLD)-- should be inserted after "Device" for clarity.

Appropriate correction is required.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject

> matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (see Fig. 3A of the drawings filed January 30, 2003 and October 27, 2003, as well as page 12, line 1 to page 14, line 23 of the specification, by way of example) in view of Buch.

With respect to claim 11, applicant's admitted prior art discloses that a passenger transit car, such as a railway passenger car or railcar, including a car drive motor, at least one solenoid, at lest one mechanical switch, and at least one motor for moving doors on the passenger transit car, was known in the art at the time the claimed invention was made. See, for example, page 12, line 1 to page 14, line 5 and Figures 3 and 3A of the present disclosure (see the drawings filed January 30, 2003).

As one of ordinary skill in the art would readily appreciate, the passenger transit car or railcar also includes an electrical control unit for controlling operation of the at least one solenoid, switch and motor to operate the doors and other parts of the railcar, the control unit having a main board or "motherboard" located within the control unit, the motherboard having at least one board. As one of ordinary skill in the art would readily appreciate, the at least one board has mounted thereon a plurality of integrated circuits or "chips" such as a microcontroller or other signal processing circuitry connected by lines or buses to process signals necessary to control the doors and other parts of the railcar in a well known manner.

The passenger transit car of applicant's admitted prior art does not include a "self-locking" data bus hold or memory circuit connected to respective bit or data lines of a tri-state data bus, so as to hold the values on the data bus at a particular value and prevent the data bus from "floating" to undetermined values and possibly causing erroneous operation by a central processing unit (CPU) or other signal processing circuitry coupled to the data bus, where the self-locking memory circuit includes a non-inverting buffer or amplifier and a resistor and changes states when a level of voltage applied thereto passes through one of upper and lower thresholds of the self-locking memory circuit.

However, Buch discloses a "self locking" memory or bus latching circuit for a tri-state data bus having multiple bit or data lines, the memory or latching circuit including a non-inverting buffer or amplifier (note 64, 66 together, e.g., in Figure 5, as well as column 5, lines 58-62) for connection to one of the bit or data lines, and a resistor (68 in Fig. 5, e.g.) having a predetermined electrical resistance connected across the buffer or amplifier. [Note that while two inverters are shown in Figure 5, Buch also teaches that a non-inverting amplifier may be used in place of the pair of inverters 64, 66 (see column 5, lines 60-62, e.g.)] The resistance value may be chosen to adjust the thresholds at which the circuit will change state. In this manner, the self-locking memory or bus latching circuit has upper and lower "threshold" voltage thresholds that cause the non-inverting buffer chip or latching circuit to change states when a level of voltage applied to the chip and the resistor "passes through" one of the thresholds. The memory or latching circuit is "self-locking" and does not change state until a voltage is again applied to the data bus which "passes through" one of the thresholds. See column 5, lines 31-

35; column 5, line 56 to column 6, line 2; column 6, line 61b to column 7, line 5; and Figure 5, for example.

Buch teaches that the bus may be a communication link between one or more computer components, and that the various components may comprise large scale integrated circuits or chips (see column 1, lines 14-39, e.g.). Bush also teaches that the components may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g.). The memory or bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level of a sufficient amount is driven onto the data bus. In this way, different components of the computer system operating at different rates may communicate over the data bus, while maintaining data integrity and allowing faster bus switching times. Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a system using "computer" components (note column 1, line 55 to column 2, line 64, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to utilize a "self-locking" memory or hold circuit as taught by Buch, on the signal lines in the passenger transit railcar of applicant's admitted prior art, in order to maintain or store the level of data on the bus until a subsequent data or voltage level of a sufficient amount is driven onto the data bus so that different components or chips operating at different rates may communicate over a data bus, while maintaining the integrity of the data on the bus and allowing faster bus switching times.

With respect to claim 12, Buch does not specifically teach that the large scale integrated circuits or chips or components of the system are comprised of a "CPU" and a "digital signal processor" (DSP) having different rates at which they operate in performing their respective functions. However, Bush does teach that the components may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g.) and, as one of ordinary skill in the art would readily appreciate, central processing units (CPUs) and digital signal processors (DSPs) are typical components used commonly with data buses.

Accordingly, it would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize the self-locking memory or bus latching circuit of Buch with large scale integrated circuit components or chips such as digital signal processors, which are components used commonly with data buses, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow fast and error free communication between the different chips. It would have been obvious to use such data bus latching circuits because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a system using "computer" components (note column 1, line 55 to column 2, line 64, e.g.).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Buch as applied to claims 11-12 above, and further in view of Chiang et al.

With respect to claim 13, applicant's admitted prior art in view of Buch discloses a passenger transit car including at least one motor, solenoid, switch and appropriate control circuits or chips, as well as a tri-state data bus and a plurality of "self-locking" data bus latching or memory circuits connected to respective bit or data lines of the data bus as in the present invention (see numbered paragraph 6 above).

Buch teaches that the "self locking" data bus latching circuit may used so that different components of a system operating at different rates may communicate over a data bus, while maintaining data integrity and allowing faster bus switching times. Buch further teaches that the bus may be a communication link between one or more computer components, and that the various components may include "nodes" comprised of large scale integrated circuits or chips including a central processing unit or CPU (see column 1, lines 14-39, e.g.), but does not specifically teach that the large scale integrated circuits or chips or components to which the bus hold circuit is connected include a complex programmable logic device (PLD) or CPLD. However, as noted above, Bush does teach that the components may comprise any typical components used commonly with data buses.

Chiang et al similarly discloses a bus hold circuit including a resistance and a non-inverting amplifier, and also teaches that the bus hold circuit may be used with busses coupled to integrated circuits, specifically teaching that the bus hold circuit may be used with complex programmable logic devices (CPLDs) to hold or latch the data on the bus (see column 1, lines 13-54 and Figure 1, e.g.).

Accordingly, it would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize large scale integrated circuit components or chips such as complex programmable logic devices, as taught by Chiang et al, which CPLDs are commonly used with data buses, in conjunction with the self-locking circuits in the passenger transit car of applicant's admitted prior in view of Buch, as discussed above, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips, including CPUs and CPLDs. It would have been obvious to use such data bus latching circuits because Buch and Chiang et al teach that the states on the data bus may be reliably held between "drives" or when the bus is not being driven but can be overwritten or overcome by the drivers to obtain a new state, and because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components (note column 1, line 55 to column 2, line 64 of Buch, e.g.), particularly one using chips such as CPUs, DSPs and CPLDs.

The reduction or avoidance of delays due to transitions in a tri-state bus and accompanying improvement in data bandwidth and integrity, coupled with the teaching of using the self-locking data bus circuit in conjunction with typical computer components and large scale integrated

circuits commonly used with data buses, as specifically taught by Buch, provide ample motivation and suggestion to utilize the self-locking data bus circuits of Buch in conjunction with computer components commonly used with data buses such as DSPs and CPLDs. One of ordinary skill in the art at the time the claimed invention was made would have found it readily obvious to utilize "typical" components such as a digital signal processor (which is merely a processor which processes digital signals) and a ("complex") programmable logic device, both of which are large scale integrated circuit components or chips commonly used with data buses, particularly in light of the specific teachings of Chiang et al.

In short, the combined teachings of the references renders obvious a structure on which applicant's claims read, and thus the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the combined teachings of the references.

6. In this regard, applicant's arguments filed May 3, 2004, have been considered, insofar as applicable, but are not persuasive.

Initially, the argument that "the hold circuit of Buch and of Figure 2 of the present invention is more susceptible to noise when it is holding the data on the data lines by itself" is not entirely understood since Figure 2 shows or describes the present invention and it is not seen how this distinguishes the teachings of Buch from the present invention. Moreover, the response does not clearly point the claim language which applicant believes is not taught by the prior art.

The structure of the claimed memory or buffer circuit [see subparagraphs A) and B) of claim 11, e.g.] is clearly taught by Buch. The language or limitation directed to the upper and lower

thresholds of the circuit [subparagraph C) of claim 11] is also taught by Buch. In this regard, the Examiner is not "relying on his own personal knowledge" regarding the threshold levels since these are taught by the prior art, and is also not invoking Official Notice that a particular claimed feature was well known in the art, since all of the claimed features are specifically taught by the prior art as discussed above.

Again, one of ordinary skill in the art provided with the teachings of Buch and having an understanding of basic electrical circuits would recognize that the "thresholds" of the self-locking memory or hold circuit may be adjusted so that the self-locking bus hold circuit changes states at desired voltage levels while certain amounts of electrical noise on the data bus will not cause the self-locking bus hold circuit and data bus to change states. Here, Buch specifically teaches that the resistance value of the memory or buffer circuit may be adjusted to protect from different levels of noise (see column 6, line 68 to column 7, line 5, e.g.) depending on the configuration used and the number and type of devices coupled to the bus. Buch further teaches that the memory buffer may be used with any typical components used commonly with data buses in computer systems (see column 3, lines 64-68 and 50-52 and column 5, lines 31-35, e.g., and also note page 7, lines 10-13 of the present specification, indicating that the buffer memory hold circuit of the present invention has utility on any data bus or digital circuit where memory of the last transfer of data requires retention and that the memory buffer can be used on any number of bit lines. Thus, the adjustment of the "thresholds" at which the buffer or latch will change states by adjusting the resistance value, and the use of such a memory buffer hold circuit on "any typical components used commonly with data buses in computer systems" is not gleaned from the examiner's "personal knowledge" or from the taking of Official Notice, but

rather is specifically taught by the prior art. Buch further teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components (again note column 1, line 55 to column 2, line 64, e.g.), highly desirable features in a computer or communication system.

The reduction in delays due to transitions on a tri-state bus, as well as the increased bus utilization and data bandwidth and improved data integrity, coupled with a direct suggestion of using the memory buffer hold circuit on any typical components used commonly with data buses in computer systems, provide ample motivation and suggestion to use such a memory buffer on the data lines or buses coupled to the components in the system of applicant's admitted prior art to arrive at a structure on which applicants' claims read. Since the claims "read on" a structure rendered obvious by the teachings of the reference, the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the prior art.

7. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187